JOO-YOUNG KIM

CONTACT INFORMATION

Affiliation:	Senior Research Hardware Design Engineer, Microsoft Research
Phone number:	+1-425-421-5344 (office) / +1-425-786-7485 (cellular)
Address:	Microsoft Corporation, One Microsoft Way, Redmond, WA 98052
E-mail:	jooyoung@microsoft.com
Web pages:	Work (http://research.microsoft.com/en-us/people/jooyoung/)
	Personal (http://hellojooyoung.com/)

RESEARCH INTERESTS

- Computer architecture and digital system design
- Hardware accelerators for cloud/mobile applications (computer vision, augmented reality, data compression, image compression, machine learning)
- Processor microarchitecture
- Low power System-on-Chip implementation

EDUCATION

Feb. 2010	**Ph.D. in Electrical Engineering (Advisor: Prof. Hoi-Jun Yoo)** **Korea Advanced Institute of Science and Technology (KAIST)** ▪ Dissertation: "High performance low power real-time multi-object recognition processor with visual perception engine"
Feb. 2007	**M.S. in Electrical Engineering and Computer Science (Advisor: Prof. Hoi-Jun Yoo)** **Korea Advanced Institute of Science and Technology (KAIST)** ▪ Dissertation: "Design of processing element and memory for pre-processing of object recognition"
Feb. 2005	**B.S. in Electrical Engineering** **Korea Advanced Institute of Science and Technology (KAIST)** ▪ Overall GPA: 3.83/4.30 (Magna cum Laude)
Feb. 2001	**Gyeonggi Science High School** ▪ 1 year early graduation

WORK EXPERIENCES

Feb.2014 – Present	**Senior Research Hardware Design Engineer, Microsoft Research,** Redmond, WA Manager: Dr. Doug Burger
Feb.2012	**Research Hardware Design Engineer III, Microsoft Research,** Redmond, WA

(2 years)	Manager: Dr. Doug Burger
Sep.2010	**Visiting Researcher, Microsoft Research,** Redmond WA
(1 year)	Manager: Dr. Doug Burger
Feb.2010	**Post-doctoral Researcher, KAIST,** Daejeon, South Korea
(8 months)	Advisor: Prof. Hoi-Jun Yoo
Jan.2006	**Research Intern, SoC Solutions,** Cerritos, CA
(3 months)	Mentor: Dr. Hyong Kim
Mar.2005	**Graduate Student, KAIST,** Daejeon, South Korea
(5 years)	Advisor: Prof. Hoi-Jun Yoo

PROJECTS

▪ **Multi GB/s data compressor (Mar. 2014-Present)**

At Microsoft Research, I am developing a high-throughput compressor that is compatible with Xpress8 compression format for in-line compression scenario such as SSD storage and networking. For multi GB/s operation, I devised a deep pipelining and multi-banking dictionary hashing scheme.

▪ **Real-time 3d reconstruction hardware (Sep. 2013-Present)**

At Microsoft Research, I am investigating a real-time camera tracking and dense 3d geometry reconstruction system with depth sensor such as Kinect or new time-of-flight camera for immersive augmented reality application. Working with computer vision scientists in Microsoft, I am architecting a vectorized accelerator to replace the current power hungry GPU implementation for mobile/client scenario.

▪ **High quality, energy efficient data compressor on FPGA (Sep. 2012 – Feb. 2014)**

At Microsoft Research, I developed a high quality and energy efficient data compressor on FPGA for large-scale data storage servers. We targeted Xpress9 compression algorithm whose compression quality is comparable with Gzip best optimization. The implemented compressor on Altera Stratix V D5 performs 1.6-2.4Gbps throughput on various compression benchmarks, supporting up to 128 thread contexts. It claims 5x better throughput and 10x lower energy than the highly optimized software running on a single Zeon core.

▪ **Real-time 6 DOF camera tracking (Sep. 2010 –Aug. 2011)**

At Microsoft Research, I created a real-time 6 degree-of-freedom camera tracking algorithm based on 2d natural feature extraction and 3d bundle adjustment. Accelerated the algorithm with graphics processing unit (GPU) utilizing CUDA parallel programming language and integrated inertial sensors such as gyroscope and accelerometer for mobile scenario.

▪ **Hyundai Motors Smart Car Project: Image Processing SoC division (Feb. 2010 –Aug. 2010)**

At KAIST, I partnered with Hyundai Motors to develop an embedded microprocessor with vector processing for Forward Collision Warning System (FCWS) and Lane Departure Warning System (LDWS). I provided the processor RTLs as well as a low-level compiler for customized instruction sets. The SoC is successfully fabricated and verified by the supporting team of the project.

▪ **BONE-V3 Vision SoC (Feb. 2007 – Jan. 2010)**

At KAIST, I led the third generation of vision SoC project consisting of 1 post-doc researcher, 3 graduate students, and 2 engineers. Architected and fabricated a 60 frame per second object recognition SoC including a specialized neural network engine and 16 vector processors in 130nm process. Demonstrated a whole vision system with the fabricated silicon as an accelerator, which also had a 640x480 video sensor, PXA270 microprocessor as a host, and Xilinx FPGA.

▪ **BONE-V1/V2 Vision SoC (Mar. 2005 – Jan. 2007)**

At KAIST, I designed a special purposed shared memory, 32b RISC processor with custom divide/logarithmic functions, and vector matching processor as an IP designer for two vision SoC projects.

▪ **ARM based multi-FPGA system (Jan. 2006 – Mar. 2006)**

At SoC Solutions, I designed an ARM based multi-media processing system on four Xilinx FPGAs.

JOURNAL & CONFERENCE PUBLICATIONS (MOST RECENT LISTED FIRST)

1. **ISCA 2014** **"A Reconfigurable Fabric for Accelerating Large-Scale Datacenter Services,"**
   Andrew Putnam, Adrian M. Caulfield, Eric S. Chung, Derek Chiou, Kypros Constantinides, John Demme, Hadi Esmaeilzadeh, Jeremy Fowers, Jan Gray, Michael Haselman, Scott Hauck, Stephen Heil, Amir Hormati, **Joo-Young Kim**, Sitaram Lanka, James R. Larus, Eric Peterson, Gopi Prashanth, Aaron Smith, Jason Thong, Phillip Yi Xiao, and Doug Burger.
   ACM/IEEE 41st Annual International Symposium on Computer Architecture (ISCA), Jun. 2014
2. **ASAP 2014** **"Energy Efficient Canonical Huffman Encoding,"**
   Janarbek Matai, **Joo-Young Kim** and Ryan Kastner
   IEEE 25th International Conference on Application-specific Systems, Architectures and Processors (ASAP), Jun. 2014
3. **FCCM 2014** **"A Scalable Multi-engine Xpress9 Compressor with Asynchronous Data Transfer,"**
   Joo-Young Kim, Scott Hauck, and Doug Burger
   IEEE 22nd International Symposium on Field-Programmable Custom Computing Machines(FCCM), May 2014
4. **JSSC 2013** **"A 320mW 342GOPS Real-Time Dynamic Object Recognition Processor for HD 720p Video Streams"**
   Jinwook Oh, Gyeonghoon Kim, Junyoung Park, Injoon Hong, Seungjin Lee, **Joo-Young Kim**, Jeong-Ho Woo, and Hoi-Jun Yoo
   IEEE Journal of Solid-State Circuits, Vol.48, No.1, Jan. 2013
5. **MICRO 2012** **"Low-Power, Real-Time Object Recognition Processor for Mobile Vision Systems"**
   Jinwook Oh, Gyeonghoon Kim, Junyoung Park, Injoon Hong, Seungjin Lee, **Joo-Young Kim**, Jeong-Ho Woo, and Hoi-Jun Yoo
   IEEE Micro, Vol.32, No.6, Nov./Dec. 2012
6. **JSSC 2012** **"A 92mW Real-Time Traffic Sign Recognition System with Robust Illumination Adaptation and Support Vector Machine"**
   Junyoung Park, Joonsoo Kwon, Jinwook Oh, Seungjin Lee, **Joo-Young Kim**, and Hoi-Jun Yoo
   IEEE Journal of Solid-State Circuits, Vol.47, No.11, Nov. 2012
7. **TNN 2011** **"24-GOPS 4.5-mm^2 Digital Cellular Neural Network for Rapid Visual Attention in an Object-Recognition SoC"**
   Seungjin Lee, Minsu Kim, Kwanho Kim, **Joo-Young Kim**, and Hoi-Jun Yoo
   IEEE Transactions on Neural Networks, Vol.22, No.1, Jan. 2011
8. **CICC 2010** **"Intelligent NoC with Neuro-Fuzzy Bandwidth Regulation for a 51 IP Object Recognition Processor,"**
   Seungjin Lee, Jinwook Oh, Minsu Kim, Junyoung Park, Joonsoo Kwon, **Joo-Young**

Kim, and Hoi-Jun Yoo
IEEE Custom Integrated Circuits Conference (CICC), Sep. 2010

9. **JSSC 2010** **"A 118.4GB/s Multi-Casting Network-on-Chip with Hierarchical Star-Ring Combined Topology for Real-Time Object Recognition,"**
Joo-Young Kim, Junyoung Park, Seungjin Lee, Minsu Kim, Jinwook Oh, and Hoi-Jun Yoo
IEEE Journal of Solid-State Circuits, Vol.45, No.7, Jul. 2010

10. **SP-IC 2010** **"An Attention Controlled Multi-Core Architecture for Energy Efficient Object Recognition"**
Joo-Young Kim, Sejong Oh, Seungjin Lee, Minsu Kim, Jinwook Oh, and Hoi-Jun Yoo
Elsevier Signal Processing: Image Communication, Vol.25, No.5, Jun. 2010

11. **VLSIC 2010** **"A 1.2mW On-Line Learning Mixed Mode Intelligent Inference Engine for Robust Object Recognition,"**
Jinwook Oh, Seungjin Lee, Minsu Kim, Joonsoo Kwon, Junyoung Park, **Joo-Young Kim**, and Hoi-Jun Yoo
IEEE Symposium on VLSI Circuits (VLSIC), June 2010

12. **COOLCHIPS 2010** **"A 36 Heterogeneous Core Architecture with Resource-Aware Fine-grained Task Scheduling for Feedback Attention based Object Recognition,"**
Seungjin Lee, Jinwook Oh, Minsu Kim, Joonyoung Park, Joonsoo Kwon, **Joo-Young Kim,** and Hoi-Jun Yoo
IEEE Symposium on Low-Power and High-Speed Chips(COOL Chips), Apr. 2010

13. **TCSVT 2010** **"Visual Image Processing RAM: Memory Architecture with 2-D Data Location Search and Data Consistency Management for a Multi-Core Object Recognition Processor"**
Joo-Young Kim, Donghyun Kim, Kwanho Kim, Seungjin Lee, and Hoi-Jun Yoo
IEEE Transactions on Circuits and Systems for Video Technology, Vol.20, No.4, Apr. 2010

14. **Pattern Recognition 2010** **"Familiarity Based Unified Visual Attention Model for Fast and Robust Object Recognition,"**
Seungjin Lee, Kwanho Kim, **Joo-Young Kim**, Minsu Kim, and Hoi-Jun Yoo
Elsevier Pattern Recognition, Vol.43, No.3, Mar. 2010

15. **JSSC 2010** "**A 201.4GOPS 496mW Real-Time Multi-Object Recognition Processor with Bio-Inspired Neural Perception Engine,"**
Joo-Young Kim, Minsu Kim, Seungjin Lee, Jinwook Oh, Kwanho Kim and Hoi-Jun Yoo
IEEE Journal of Solid-State Circuits, Vol.45, No.1, Jan. 2010

16. **MICRO 2009** "**Real-Time Object Recognition with Neuro-Fuzzy Controlled Workload-aware Task Pipelining,"**
Joo-Young Kim, Minsu Kim, Seungjin Lee, Jinwook Oh, Sejong Oh, and Hoi-Jun Yoo
IEEE Micro, Vol.29, No.6, Nov./Dec. 2009

17. **TCSVT 2009** **"A Configurable Heterogeneous Multicore Architecture with Cellular Neural Network for Real-Time Object Recognition,"**
Kwanho Kim, Seungjin Lee, **Joo-Young Kim**, Minsu Kim, and Hoi-Jun Yoo
IEEE transactions on circuits and systems for video technology, Vol. 19, No. 11, Nov. 2009

18. **IET-CDT 2009** **"Memory-Centric Network-on-Chip for Power Efficient Execution of Task-Level Pipeline on a Multi-Core Processor,"**
Kwanho Kim, Seungjin Lee, **Joo-Young Kim**, Minsu Kim, and Hoi-Jun Yoo
IET Computers & Digital Techniques, Vol. 3, No. 5, Sep. 2009

19. **ESSCIRC 2009** **"A 118.4GB/s Multi-Casting Network-on-Chip for Real-Time Object Recognition Processor,"**
Joo-Young Kim, Kwanho Kim, Minsu Kim, Seungjin Lee, Jinwook Oh, and Hoi-Jun Yoo
IEEE European Solid-State Circuits Conference (ESSCIRC), Sep. 2009

20. **ISLPED 2009** **"A 60fps 496mW Multi-Object Recognition Processor with Workload-Aware Dynamic Power Management,"**

Joo-Young Kim, Seungjin Lee, Jinwook Oh, Minsu Kim, and Hoi-Jun Yoo
ACM/*IEEE International Symposium on Low Power Electronics and Design (ISLPED), Aug. 2009*

21. **VLSIC 2009** "**A 22.8GOPS 2.83mW Neuro-fuzzy Object Detection Engine for Fast Multi-object Recognition,"**
Minsu Kim, **Joo-Young Kim,** Seungjin Lee, Jinwook Oh, and Hoi-Jun Yoo
IEEE Symposium on VLSI Circuits (VLSIC), June 2009

22. **COOLCHIPS 2009** "**An Energy Efficient Real-Time Object Recognition Processor with Neuro-Fuzzy Controlled Task Pipelining,"**
Joo-Young Kim, Minsu Kim, Seungjin Lee, Jinwook Oh, Kwanho Kim, and Hoi-Jun Yoo
IEEE Symposium on Low- Power and High-Speed Chips (COOL Chips), Apr 2009

23. **TVLSI 2009** **"81.6 GOPS Object Recognition Processor Based on a Memory-Centric NoC,"**
Donghyun Kim, Kwanho Kim, **Joo-Young Kim**, Seungjin Lee, Se-Joong Lee, and Hoi-Jun Yoo
IEEE Transactions on Very Large Scale Integration, Vol.17, No.3, Mar. 2009

24. **ISSCC 2009** "**A 201.4GOPS 496mW Real-Time Multi-Object Recognition Processor with Bio-Inspired Neural Perception Engine,"**
Joo-Young Kim, Minsu Kim, Seungjin Lee, Jinwook Oh, Kwanho Kim, Sejong Oh, Jeong-Ho Woo, Donghyun Kim, and Hoi-Jun Yoo,
IEEE International Solid-State Circuits Conference (ISSCC), Feb 2009

25. **JSSC 2009** **"A 125 GOPS 583 mW Network-on-Chip Based Parallel Processor with Bio-Inspired Visual Attention Engine,"**
Kwanho Kim, Seungjin Lee, **Joo-Young Kim**, Minsu Kim, and Hoi-Jun Yoo
IEEE Journal of Solid-State Circuits, Vol.44, No.1, Jan. 2009

26. **A-SSCC 2008** "**A 66fps 38mW Nearest Neighbor Matching Processor with Hierarchical VQ Algorithm for Real-Time Object Recognition,"**
Joo-Young Kim, Kwanho Kim, Seungjin Lee, Minsu Kim, and Hoi-Jun Yoo
IEEE Asian Solid-State Circuits Conference (A-SSCC), Nov 2008

27. **A-SSCC 2008** "**A 76.8 GB/s 46 mW Low-latency Network-on-Chip for Real-time Object Recognition Processor,"**
Kwanho Kim, **Joo-Young Kim,** Seungjin Lee, Minsu Kim, and Hoi-Jun Yoo
IEEE Asian Solid-State Circuits Conference (A-SSCC), Nov 2008

28. **ESSCIRC 2008** **"A 211 GOPS/W Dual-Mode Real-Time Object Recognition Processor with Network-on-Chip,"**
Kwanho Kim, **Joo-Young Kim,** Seungjin Lee, Minsu Kim, and Hoi-Jun Yoo
IEEE European Solid-State Circuits Conference (ESSCIRC), Sep 2008

29. **VLSIC 2008** "**The Brain Mimicking Visual Attention Engine: An 80x60 Digital Cellular Neural Network for Rapid Global Feature Extraction,"**
Seungjin Lee, Kwanho Kim, Minsu Kim, **Joo-Young Kim,** and Hoi-Jun Yoo
IEEE Symposium on VLSI Circuits (VLSIC), June 2008

30. **DAC 2008** **"Vision Platform for Mobile Intelligent Robots Based on 81.6 GOPS Objects Recognition Processor,"**
Donghyun Kim, Kwanho Kim, **Joo-Young Kim,** Seungjin Lee, and Hoi-Jun Yoo
ACM Design Automation Conference (DAC), June 2008

31. **ISCAS 2008** "**A 0.6pJ/b 3Gb/s/ch Transceiver in 0.18 um CMOS for 10mm On-chip interconnects,"**
Joonsung Bae, **Joo-Young Kim,** and Hoi-Jun Yoo
IEEE International Symposium on Circuit and Systems (ISCAS), May 2008

32. **ISSCC 2008** "**A 125GOPS 583mW Network-on-Chip Based Parallel Processor with Bio-inspired Visual Attention Engine,"**
Kwanho Kim, Seungjin Lee, **Joo-Young Kim,** Minsu Kim, Donghyun Kim, Jeong-Ho Woo, and Hoi-Jun Yoo,
IEEE International Solid-State Circuits Conference (ISSCC), Feb 2008

33. **A-SSCC 2007** "**Bitwise Competition Logic for Compact Digital Comparator,"**
Joo-Young Kim, and Hoi-Jun Yoo

IEEE Asian Solid-State Circuits Conference (A-SSCC), Nov 2007

34. **A-SSCC 2007** "**Implementation of Memory-Centric NoC for 81.6 GOPS Object Recognition Processor,"**
Donghyun Kim, Kwanho Kim, **Joo-Young Kim,** Seungjin Lee, and Hoi-Jun Yoo
IEEE Asian Solid-State Circuits Conference (A-SSCC), Nov 2007

35. **ESSCIRC 2007** "**Visual Image Processing RAM for Fast 2-D Data Location Search,"**
Joo-Young Kim, Donghyun Kim, Seungjin Lee, Kwanho Kim, and Hoi-Jun Yoo
IEEE European Solid-State Circuits Conference (ESSCIRC), Sep 2007

36. **CICC 2007** **"An 81.6 GOPS Object Recognition Processor Based on NoC and Visual Image Processing Memory,"**
Donghyun Kim, Kwanho Kim, **Joo-Young Kim,** Seungjin Lee, and Hoi-Jun Yoo
IEEE Custom Circuits Conference (CICC), Sep 2007

37. **NOCS 2007** **"Solutions for Real Chip Implementation Issues of NoC and Their Application to Memory-Centric NoC,"**
Donghyun Kim, Kwanho Kim, **Joo-Young Kim,** Seungjin Lee, and Hoi-Jun Yoo
IEEE International Symposium on Network-on-Chip (NOCS), May 2007

38. **ISCAS 2006** "**A 372ps 64-bit Adder using Fast Pull-up Logic in 0.18-um CMOS,"**
Joo-Young Kim, Kangmin Lee, and Hoi-Jun Yoo
IEEE International Symposium on Circuit and Systems (ISCAS), May 2006

39. **A-SSCC 2006** **"A TCAM-based Periodic Event Generator for Multi-Node Management in the Body Sensor Network,"**
Sungdae Choi, Kyomin Sohn, **Jooyoung Kim**, Jerald Yoo, and Hoi-Jun Yoo
IEEE Asian Solid-State Circuits Conference (A-SSCC), Nov. 2006

40. **A-SSCC 2006** **"A 0.6-V, 6.8-uW Embedded SRAM for Ultra-low Power SoC,"**
Kyomin Sohn, Sungdae Choi, Jeong-Ho Woo, **Jooyoung Kim**, and Hoi-Jun Yoo
IEEE Asian Solid-State Circuits Conference (A-SSCC), Nov. 2006

41. **ESSCIRC 2006** **"A 24.2-uW Dual-Mode Human Body Communication Controller for Body Sensor Network,"**
Sungdae Choi, Seong-Jun Song, Kyomin Sohn, Hyejung Kim, **Jooyoung Kim**, Namjun Cho, Jeong-Ho Woo, Jerald Yoo and Hoi-Jun Yoo
IEEE European Solid-State Circuits Conference(ESSCIRC), Sep. 2006

42. **CICC 2006** **"A Multi-Nodes Human Body Communication Sensor Network Control Processor,"**
Sungdae Choi, Seong-Jun Song, Kyomin Sohn, Hyejung Kim, **Jooyoung Kim**, Namjun Cho, Jeong-Ho Woo, Jerald Yoo and Hoi-Jun Yoo
IEEE Custom Circuits Conference (CICC), Sep. 2006

43. **ISWC 2006** **"A Low-power Star-topology Body Area Network Controller for Periodic Data Monitoring Around and Inside the Human Body ,"**
Sungdae Choi, Seong-Jun Song, Kyomin Sohn, Hyejung Kim, **Jooyoung Kim**, Jerald Yoo, and Hoi-Jun Yoo
IEEE International Symposium on Wearable Computers (ISWC), June 2006

HONORS

- **Design Contest Winner, *Design Automation Conference 2010***

  "A Real-time Embedded Vision System with 201.4GOPS 496mW Object Recognition Processor,"

  Joo-Young Kim, Seungjin Lee, Minsu Kim, Jinwook Oh, and Hoi-Jun Yoo

- **Design Contest Winner, *Design Automation Conference 2008***

  "Vision Platform for Mobile Intelligent Robot based on 81.6GOPS Object Recognition Processor,"

  Donghyun Kim, Kwanho Kim, **Joo-Young Kim**, Seungjin Lee, and Hoi-Jun Yoo

- **Design Contest Winner, *Asian Solid State Circuits Conference 2006***

  "A TCAM based Periodic Event Generator for Multi-node Management in Body Sensor Network,"

Sungdae Choi, Kyomin Sohn, **Joo-Young Kim**, Jerald Yoo

PROFESSIONAL ACTIVITIES

▪ Technical Program Committee for HEART 2014

▪ Technical Committee Chair at KAIST EE-CS joint workshop, Jan. 2012

▪ Technical Committee Chair at KAIST-Keio-Tsinghua (KKT) workshop, Aug. 2009

▪ Invited talks

- Talk on hardware accelerators at North West Regional Conference 2013, Seattle, WA (Sep 2013)
- Talk on 6-DOF camera tracking at Chung-Nam National University, Daejeon, South Korea (Dec 2011)
- Talk on BONE-V3 Vision SoC at Intel, Santa Clara, CA (Aug 2009)
- Talk on BONE-V3 Vision SoC at nVidia, Santa Clara, CA (Aug 2009)
- Talk on BONE-V3 Vision SoC at Texas Instruments, Dallas, TX (Aug 2009)
- Talk on BONE-V3 Vision SoC at IMEC, Leuven, Belgium (Sep 2009)
- Talk on BONE-V3 Vision SoC at Technical University of Eindhoven, Eindhoven, Netherlands (Sep 2009)

▪ External Reviewer

IEEE JSSC, IEEE ISSCC, IEEE TCAS, IEEE TCAS-II, IEEE VLSIC, IEEE A-SSCC, ACM/IEEE NOCS, IEEE ISCAS, IEEE VLSI-DAT

PERSONAL

▪ Korean as a mother tongue / fluent English

▪ U.S. green card holder

REFERENCES

▪ Available upon request