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Implementation of Memory-Centric NoC for 81.6 GOPS Object Recognition Processor

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***Abstract* –An 81.6 GOPS object recognition processor based on Memory-Centric NoC (MC-NoC) is implemented in a 0.18-µm CMOS technology. The MC-NoC facilitates data transactions among 10 SIMD Processing Elements (PEs) by exploiting 8 Visual Image Processing (VIP) memories. The 10 PEs implement special SIMD instructions to perform Gaussian filtering at 16 GOPS. The 8 VIP memories provide one cycle local maximum pixels search operation performing 65.6 GOPS. The chip dissipates 1.4W at 200 MHz operating frequency.**

I. INTRODUCTION

Object recognition has wide range of applications such as vehicle detection in driver assistant system or vision based navigation of intelligent robots [1-3]. High computing power is generally required for the object recognition because their image processing stage relies on heavy iterations of pixel calculation. In addition, low power consumption is more emphasized for intelligent robots compared to the other applications due to their limited power supply. In the perspective of power consumption, conventional processor is not appropriate as it dissipates ~13W, which is more than 50% of total robot power [4]. Therefore, dedicated processor implementation with reasonable performance and power consumption is demanded for the object recognition in robot applications.

In many cases, Scale Invariant Feature Transform (SIFT) based object recognition [5] is used for intelligent robot applications [6, 7], which is also base of our processor implementation. Because of high computation requirement of the SIFT, chip multi-processor design is adopted for the proposed object recognition processor. In recent years, high computing power is generally provided by number of processing elements distributed on a chip because of poor scalability and inefficiency of single wide-issue processors [8]. Efficient computation of the SIFT can be achieved by exploiting data and task level parallelism. In the proposed processor, data level parallelism is supported by addition of SIMD instruction to the Processing Elements (PEs) whereas task level parallelism is available by integrating multiple PEs for parallel execution of the SIFT tasks. Because of interactions between the tasks, however, sophisticated communication scheme among PEs is also necessary to exploit task level parallelism efficiently. In the proposed object recognition processor, Memory Centric Networks-on-Chip (MC-NoC) provides parallel communication channels among PEs by managing distributed shared memories which are dynamically assigned to the PEs involved in data transaction.

This paper describes details of the MC-NoC implementation for 81.6 GOPS object recognition processor. Main processing components of the proposed processor are SIMD PEs and Visual Image Processing (VIP) Memories which contribute 16GOPS and 65.6 GOPS of the total performance respectively. For efficient use of the processing components, the MC-NoC provides dynamic shared memory communication channels to the sub-sets of PEs and also supports data synchronization schemes among them.

The rest of the paper is organized as follows. In section 2, data transaction characteristics of the SIFT computation is described. Then, section 3 describes the architecture and operation of the MC-NoC whereas section 4 details the SIMD PE and the VIP memory. Performance evaluation and implementation results will be shown in section 5. Finally, summary and conclusion of the paper is made in section 6.

II. CHARACTERISTICS OF DATA TRANSACTIONS

Scale Invariant Feature Transform (SIFT) is the process of generating descriptor vectors from input image data. These vectors represent features of object and used by subsequent classifiers to perform object recognition [5]. Computation of the SIFT is mainly divided into key-point localization and descriptor vector generation stages. In this section, we focus on key-point localization stage of the SIFT because data transactions between tasks are heavily occur in the key-point localization stage. Fig. 1 shows the overall flow of the computation and data transactions.

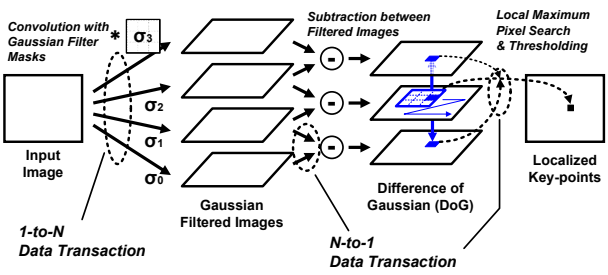

Figure 1. Overall Flow of the SIFT Computation

For key-point localization, Gaussian filtering with varying coefficients is repeatedly performed on input image. Then subtractions among the filtered images are carried out to yield Difference of Gaussian (DoG) images. Locations of key-points are decided by finding local maximum values using a 3x3 search window over entire DoG images. The pixels holding local maximum value greater than given threshold become key-points. The number of key-points detected in a single input image is about few hundreds. Characteristics of data transactions between the SIFT tasks are summarized as follows.

1) *Uni-directional data flow among tasks*
2) *1-to-N or N-to-1 data transactions to exchange intermediate result among the SIFT tasks.*

Therefore, we propose the Memory-Centric NoC (MC-NoC) which efficiently supports data transactions characteristics listed above. Architecture and operation of the MC-NoC is described in the next section.

III. MEMORY-CENTRIC NOC

Fig. 2 shows architecture of the proposed object recognition processor based on the MC-NoC. The MC-NoC consists of 8 VIP memories and 5 crossbar switches which are interconnected in hierarchical star topology. The other building blocks of the MC-NoC are Network Interface (NI), and channel controllers. Under the management of the channel controllers, the VIP memories are dynamically assigned to the PEs as a communication channel among them. Then, data transactions between tasks are performed by accessing the assigned VIP memory. In the MC-NoC, dual port design is adopted for the VIP memory to facilitate simultaneous data access and to provide data transfer channels between left and right side of the processor. For efficient link utilization, the MC-NoC implements packet switching network whereas operation frequency of the crossbar switches is designed to be twice of the other part of the MC-NoC to reduce latency overhead of packet switching. The NI performs packet processing and clock synchronization between crossbar switch and other building blocks of the MC-NoC.

Fig. 3 briefly describes important step of the MC-NoC operation. In this figure, crossbar switches are not drawn for simplicity. While the operation is explained, we will assume that PE0 sends processed results to the PE 2 and PE3. The MC-NoC operation is initiated by PE0 sending *Open Channel* request to the channel controller. The information about source and destination PEs is defined in the *Open Channel* request. After that, channel controller assigns one VIP memory as a data communication channel if any of the VIP memory is not used by other PEs. By updating routing Look Up Tables (LUTs) in NIs of corresponding PEs, VIP memory assignment is accomplished. In this way, assigned VIP memory is made to be accessible only for the PEs involved in data transaction – namely PE0, 2, and 3. At the end of the data transaction, source PE send *Close Channel* request to the channel controller. Then, channel controller invalidate updated

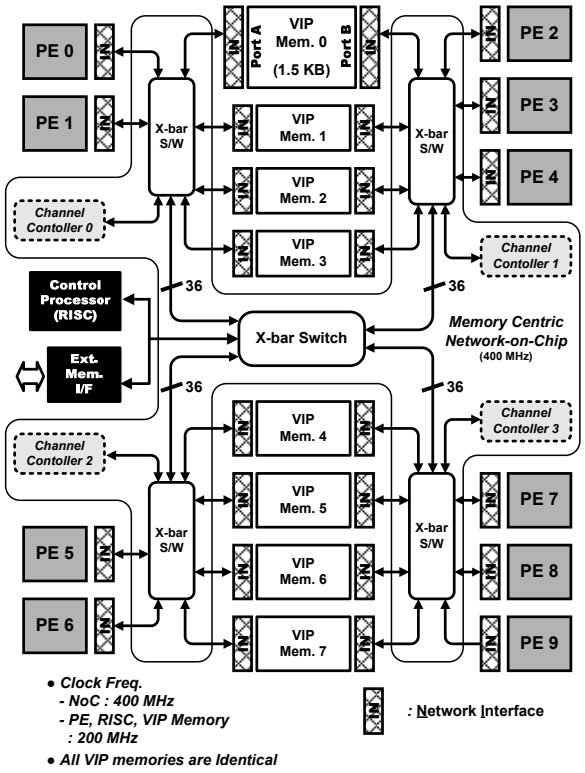

Figure 2. Architecture of the Proposed Object Recognition Prcoessor based on the MC-NoC

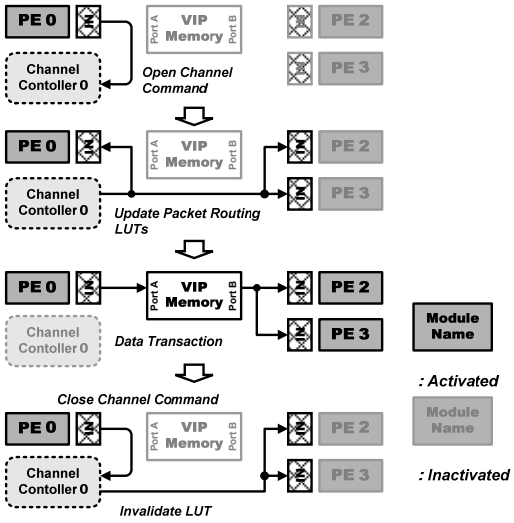

Figure 3. Operation of the MC-NoC

LUTs after checking completion of reading data from source PEs. In the proposed MC-NoC, each PE is able to send multiple *Open Channel* request as required. If all the VIP memories are used by other PEs the data transaction should be stalled until one of the VIP memories become available.

Since most of the data transactions are unidirectional as shown in section II, data synchronization scheme for 1-to-N unidirectional data flow is also implemented in the MC-NoC.

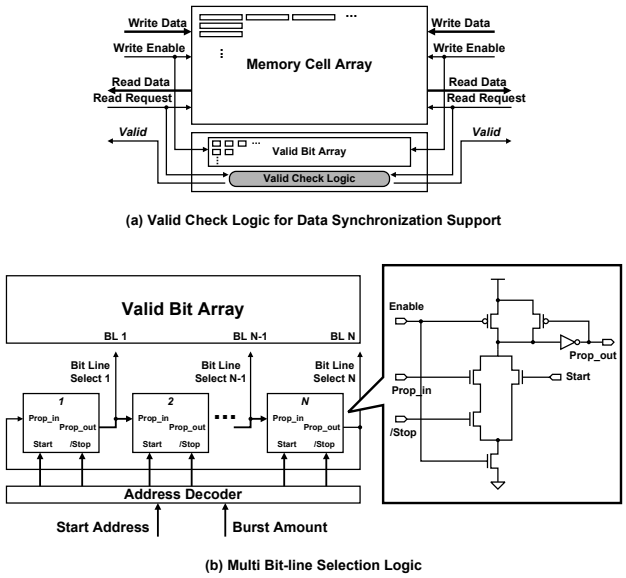

Figure 4. Valid Check Logic of the VIP Memory for Data Synchronization

In the MC-NoC, unidirectional data synchronization is supported by additional valid check logic inside the VIP memory. Once the VIP memory is assigned for communication among PEs, the VIP memory checks every write into the memory cell array by also writing '1' to the corresponding single bit of the valid bit array as shown in Fig. 4 (a). In case of reading the VIP memory, valid check logic indicates whether requested data is valid or not. Based on the valid check result, the MC-NoC holds reading PEs until valid data is written into the VIP memory. In programmer's view, this removes overhead of adding waiting loop for valid data in the receiver PE. More detailed operation of the data synchronization is described in [9]. Because the MC-NoC supports burst read operation, selecting multiple subsequent cells in valid bit array is necessary. Fig. 4 (b) shows the proposed multi-bit line selection logic. Using start/stop signals and cascaded domino logic, the proposed circuit generates simultaneous 16 bit line selection signals in 0.7 ns.

IV. SIMD PE AND VIP MEMORY

Pre-design analysis on the SIFT object recognition is carried out to decide architecture of the processor. Since 54% and 22% of computing power is required for Gaussian filtering and local maximum pixel search operation respectively, we decided to implement SIMD PE and the VIP memory to accelerate the corresponding tasks. This section describes SIMD PE and VIP memory in detail.

1) SIMD PE

Because Gaussian filtering involves intensive computation, special instructions for image filtering are implemented in the PE. The instructions are SDP (Sum of Dot Product) and LE (Load Extension). The SDP instruction calculates 8 bit 4-way SIMD multiplications and subsequent 4 additions including accumulation in a single cycle. The LE instruction is combination of 8 bit shift and byte load operation, which is designed to supports seamless filtering window movement over image data. By performing the SDP instruction, the PE performs 8 operations in one cycle, where its operation frequency is 200 MHz. As a result, the 10 PEs contributes to 16 GOPS of the total performance.

2) Visual Image Processing Memory

The VIP memory is specially designed to find location of local maximum pixel inside 3x3 search window in a single cycle. According to the location of the local maximum pixel searching operation needs 29~53 cycles on ARM based RISC processor. By replacing this time consuming computation with single read operation, huge performance gain is obtained for key-point localization task. Since local maximum pixel search operation takes 41 cycles on average, 8 VIP memories operating at 200MHz give 65.6 GOPS performance gain.

Fig. 5 shows overall architecture of the VIP memory. In the VIP memory, 12 rows by 32 columns of 32 bit pixels are stored which result in total 1.5KB capacity. To compare 9 pixel values in one cycle, every row is interleaved into 3 banks so that bank number assigned for each row is decided by Mod3 operation. Three pixels in the same row are first compared inside the bank, then results from 3 banks are compared again to find local maximum pixel among 9 pixels. Address of local maximum pixel is automatically generated according to the comparison result by address generation unit. At each banks, 3 Comparison Amplifiers (CA) are integrated into every 4 bit line pairs to read 3 pixel values simultaneously. The transistor size of the CA is smaller than normal sense amplifier because it does not drives capacitive long DB lines.

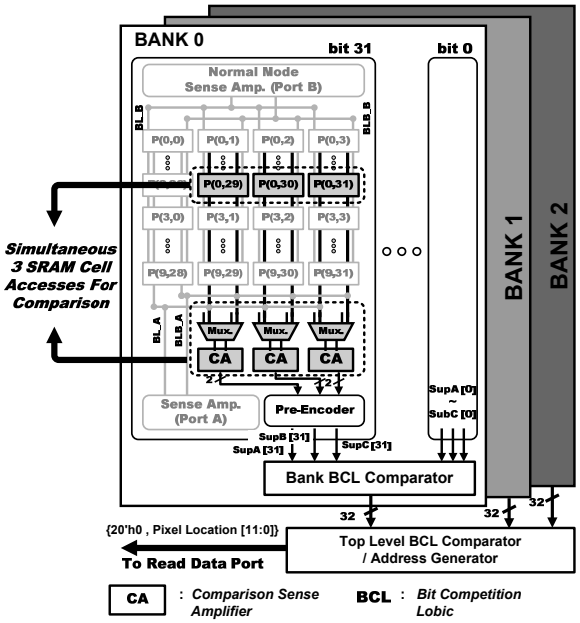

Figure 5. Overall Architecture of the VIP memory

To reduce area overhead of comparison logic, Bit Competition Logic (BCL) is also devised. By using priority coded sequential pull down logic, transistor count of the BCL is reduced from 2400 to 536 when compared to the conventional adder based comparator.

V. Performance Evaluation Results

To evaluate performance, we mapped key-point localization tasks of the SIFT to the proposed processor. Input image, whose size is 320 x 240 pixels, is divided into 32 x 12 pixel sub-images to fit into the VIP memory size. Fig. 6 illustrates cycle count required to perform key-point localization on a sub-image. The SDP/LE instructions and the VIP memory contribute to reduce execution cycles from 94,204 to 30,904. Table 1 depicts performance comparisons with the previous works. When we compare GOPS/W, the proposed processor shows at least 3.2 times improvement over previous implementations. This power efficiency is obtained from the VIP memory, which removes power consumed for numerous memory accesses and computing cycles by replacing them with a single VIP memory read operation.

Fig. 7 summarizes implementation results. Gate count breakdown is also shown to indicate overhead of the Memory Centric NoC. The gate count breakdown is calculated excluding the 8 1.5KB VIP memories. The proposed object recognition processor is implemented with 0.18um 1-poly 6-metal standard CMOS process. Operation frequency of the chip is 400 MHz for the NoC and 200 MHz for the other part of the chip. Size of the chip is 7.7mm x 5mm and its peak power consumption is 1.4W.

VI. Colclusion

In this paper, we proposed an 81.6 GOPS object recognition processors based on Memory-Centric NoC. The 10 PEs and 8 VIP memories contributes 16GOPS and 65.6 GOPS performance respectively. This huge performance comes from the special image filtering instructions and active utilization of the VIP memory, while the MC-NoC facilitates

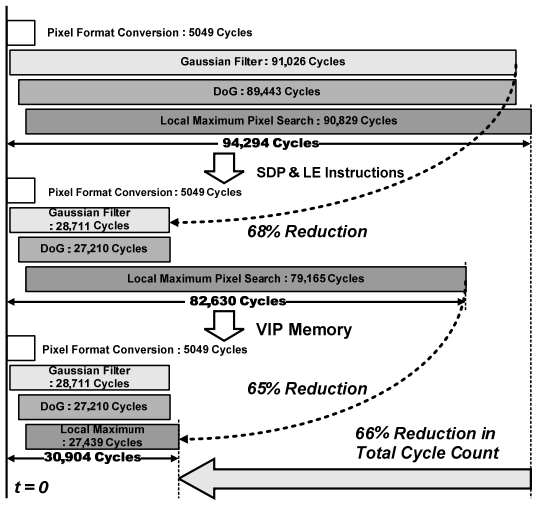

Figure 6. Performance Evaluation Results of Key-point Localization

TABLE I. Performance Comparison with Previous Works

	IMAP-CE [1]	VIP [2]	Visconti [3]	This Work
Peak GOPS	51.2	53	18	**81.6**
Power	4W (1.8V)	8W (3.3V)	1W (1.5V)	1.4W (1.8V)
Area (mm^2)	121	506	48.7	38.5
GOPS/W	12.8	6.63	18	**58.3**

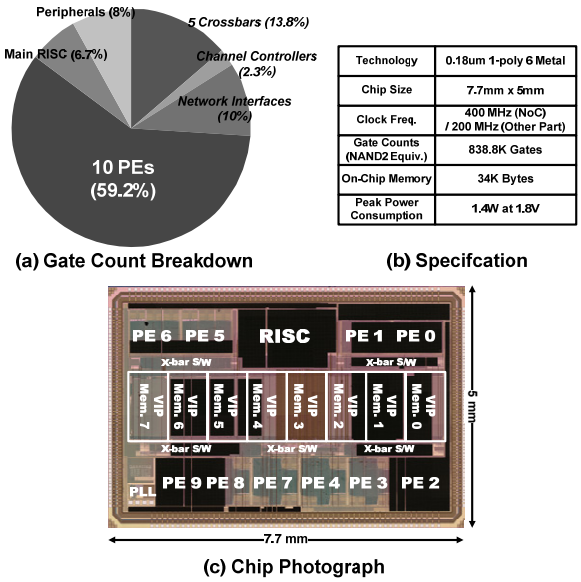

Figure 7. Implementation Results

data transactions among parallel tasks. High power efficiency of the proposed processor is suitable for intelligent robots equipped with limited power supply.

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