A 24.2-μW Dual-Mode Human Body Communication Controller for Body Sensor Network

Sungdae Choi, Seong-Jun Song, Kyomin Sohn, Hyejung Kim, Jooyoung Kim, Namjun Cho, Jeong-Ho Woo, Jerald Yoo and Hoi-Jun Yoo
Semiconductor System Laboratory, Department of EECS
Korea Advanced Institute of Science and Technology
Daejeon, Korea.
(next@eeinfo.kaist.ac.kr)

Abstract— **The human body communication (HBC) system needs a low power controller to build a body sensor network (BSN). This paper presents a system architecture with low-power consumption to manage 254 nodes in the BSN. Its 'instantaneous program execution with external program counter' scheme prohibits unnecessary RISC operation and 'TCAM-based period scheduler' structure manages 254 periods information of each network node with low energy consumption. The test chip consumes 24.2-μW for 254 nodes management and 4.2-MIPS performance.**

I. INTRODUCTION

The increasing concern about the healthcare and well-being brought up the research of mobile medical service [1] and body sensor network (BSN) so that people can check their own health conditions at any time and any place. In the mobile medical service applications such as remote healthcare monitoring and diagnostics, functions of collecting and analyzing a number of vital signs from different parts of a human body are essential. And ultra low-power consumption is also one of the most crucial requirements for the implantable system which needs surgical operations and cannot be recharged after it is implanted inside human body. Its low-power consumption can reduce the size of battery, resulting in small system form-factor.

Various BSN systems were proposed [2, 3] to implement a mobile healthcare monitoring system. A handheld device like a PDA is used for a network manager or a base-station to manage all the sensor nodes and handle events with its CPU [2]. However, its large form-factor and big battery due to its large power consumption are inconvenient for users to carry with. Although another system with general purpose microcontroller was introduced for low-power operation [3], it can control just 3~4 directly connected sensor nodes, which cannot provide the performance for network management. And most of them use wireless communication which consumes more power than human body communication (HBC) [4].

This paper presents a new hardware architecture and its chip implementation for ultra low-power BSN control. It uses HBC scheme for the communication among the nodes. HBC consumes less power than other wireless schemes and is suitable for BSN because most sensors are directly connected with or implanted inside the human body.

II. BODY SENSOR NETWORK CONTROLLER

Figure 1 shows the state diagram of the operations of the BSN controller. It starts the whole network system including each network node with the system initialization. And it periodically requests the sensor data and stores them in its internal memory for monitoring the status of the human body. If some of the incoming data include warning information or values exceeding pre-defined boundary, it switches to the analysis routine or therapy routine to resolve the problem.

Such operations can be grouped into two operation categories: category 1 - 'simple but frequently occurred operations' such as data-request with scheduled period, and category 2 - 'complex but rarely occurred operations' such as alert handling in the figure 1. Category 1 occurs in real-time to gather the sensor data, and the period of the data-request depends on the characteristics of the sensor. For example, a body temperature should be gathered every 2-minutes while a blood pressure should be checked three times a day. From the view point of CPU clock, such period is too long to count, and counting the period by using the CPU is waste of performance and power. Category 2 occurs when incoming data has abnormal condition or exceeds the pre-defined safety range, and needs high computing performance to execute analysis/therapy programs. Conventional architecture with general purpose CPUs [5] uses interrupt service routines (ISR) to handle exceptions. However, they have only limited number of interrupt resources to allocate to each node. Although the number can be extended by using interrupt controller, extra operations for interrupt request (IRQ) analysis requires additional execution time and power consumption.

In conventional architectures, operations of both categories were handled by a general-purpose CPU which cannot provide any optimized operations to any of the categories. The proposed architecture, meanwhile, is divided into two operation modes to manage 254 BSN nodes with 24.2-μW power consumption. A schedule director (SD) with ternary content addressable memory (TCAM)-based periodic event generator (PEG) manages the issuing period for each node with 16-kHz clock frequency. The instantaneous program execution with external program counter (IPEEP) scheme activates the CPU only when it is needed.

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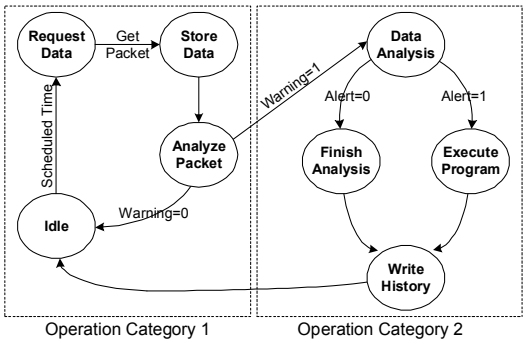

Figure 1. Operations for Body Sensor Network Management

III. PROPOSED BSN SYSTEM ARCHITECTURE

The proposed system is composed of two modules, the performance-aware module and the energy-aware module, as shown in figure 2. The RISC is the master of the system bus and memory blocks, but it is activated by SD. For periodic data request operations, only the energy-aware module is activated and SD itself controls the whole system. When complex jobs should be executed, SD wakes up the RISC. Then the performance-aware module is activated and the RISC controls the whole system.

Average power dissipation of the entire system depends on the activation ratio of the RISC which consumes most of the system power and the clock frequency. Due to the proposed TCAM-based PEG, SD works with as low as 16-kHz clock frequency to reduce the number of signal transitions and corresponding charging and discharging power consumption. The proposed IPEEP scheme activates the performance-aware module without operational overhead such as register backup and restoration. Assuming that the RISC is activated one minute per every hour, the activation ratio is just 1.7% and the whole system power consumption can be dramatically reduced by selectively activating the performance-aware module only when it is needed.

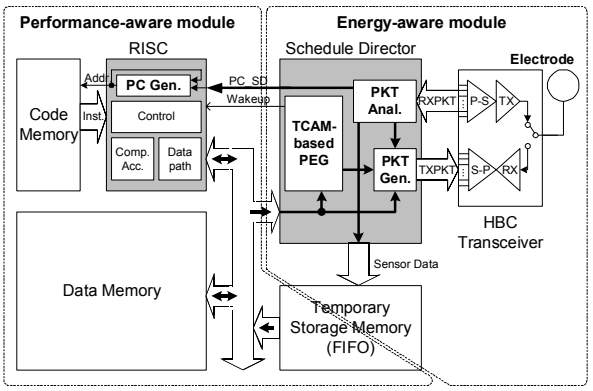

Figure 2. BSN Controller Architecture for Dual-mode Operations

A. TCAM-based Periodic Event Generator

SD manages outgoing data-request/command packets and incoming data from each BSN node. The TCAM-based PEG issues and generates data-request packets with up to 254 independent periods for BSN nodes, while conventional system issues them using hardware timers which consume considerable power and silicon area. It is one of the reasons why conventional CPU supports only limited number of timers.

In the CAM operation, most of energy is consumed for search operation. In this application, however, search operation occurs just once a second and it finds out the ID of the nodes to be issued by enabling corresponding match lines (ML). The search results are issued in order, from ML1 to MLn, by the Request Generation block with 16-kHz clock frequency as shown in figure 3 (a). If a ML is enabled, the generation block issues the data-request packet by using the row number as the node number. And if the ML is disabled, it skips the packet generation and checks next ML. Figure 4 compares the energy consumption of the conventional hardware timer and the proposed PEG with three values of TCAM match ratio. If the CAM searches 10 match lines out of 256 words every search cycle, the ratio becomes 4%. It shows that the TCAM-based PEG consumes 8x less energy for management of 100 nodes.

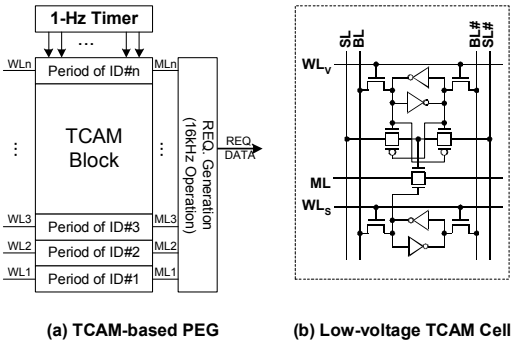

Figure 3. TCAM-based PEG

Figure 3 (b) shows the proposed 18-Tr. NAND-type TCAM cell for low voltage search operation. Although it has two more pMOS transistors compared with previous NAND-type TCAM cell [6], the transmission gate passes the match signal without Vth-drop, which enables 0.6V supply voltage search operation.

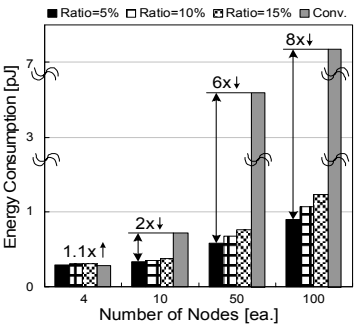

Figure 4. Energy Consumption for Scheduling Nodes

Bit ordering of the search data affects the search energy consumption of the NAND-type CAM. The timer block in PEG generates the search data based on the real-time and the value increases linearly. The NAND-type CAM compares each bit sequentially, from MSB to LSB. If MSB mismatches, the CAM consumes less energy than the mismatch with LSB because the loading capacitance of the match line (ML) decreases. We can reduce the ML energy consumption by allocating frequently changing bit to MSB of the CAM. Figure 5 shows the search power consumption of the CAM blocks with and without the bit order consideration. In the figure 5, the block with bit-order consideration consumes 61% power of the block without it.

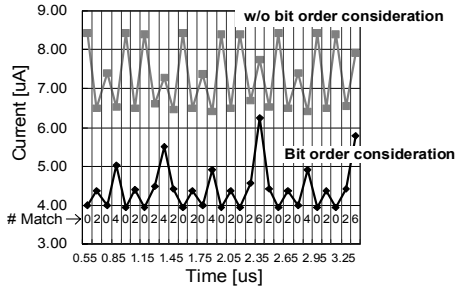

Figure 5. Comparison of Search Power

B. *Direct Program Execution Scheme*

Two kinds of resets exist in the proposed IPEEP scheme, resets by external reset-switch and by SD. With the system start-up, the RISC executes a program starting from the address 0, in which generally the instructions for system initialization or boot-up are stored. With the IPEEP scheme, end of the boot-up instructions includes the CPU power-save mode instruction so that the RISC cuts off its power autonomously to reduce both the dynamic power and leakage power. When SD wakes up the RISC, it provides an appropriate program counter (PC) value and the RISC executes a program starting from the address pointed by the PC. Since internal registers of the RISC is initialized by the same way as the conventional reset sequence, additional time for restoring internal registers or IRQ handling is not required. With the IPEEP scheme, large number of interrupt handling is achieved without interrupt control IP and ISR. For the realization of IPEEP scheme, the PC generation block of the RISC has two PC inputs, internal PC and external PC. And SD generates the wake-up signal by analyzing the incoming data packets.

Figure 6 shows an example of the memory map with IPEEP scheme for a healthcare monitoring system. With the system reset, the initialization code sets all of the BSN system as well as each node and it goes to power-save mode, and SD manages all the sensor nodes. When SD gets abnormal sensor data, it wakes up the RISC with PC2 and the RISC executes symptom analysis program. And when SD gets alert signal from a sensor node, it wakes up the RISC with PC1 so that the RISC executes therapy program. After the RISC completes the program execution, it goes to the power-save mode and cuts off its power.

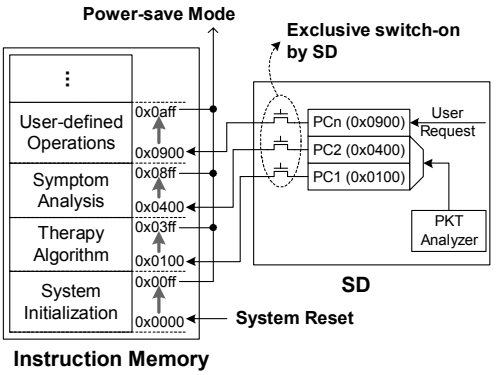

Figure 6. PC Transition with IPEEP Scheme

IV. IMPLEMENTATION RESULTS

The proposed architecture is implemented for an ultra low-power HBC BSN control processor as shown in figure 7. The 25mm^2 chip consists of a 16bit RISC with IPEEP scheme, SD, three application-specific memory blocks and the HBC transceiver. Data I/O interface of SD is designed to communicate with simplified packet structure so that it can easily connect with HBC transceiver. The processor is implemented with 0.18-μm CMOS logic process and it works with 0.6V core voltage.

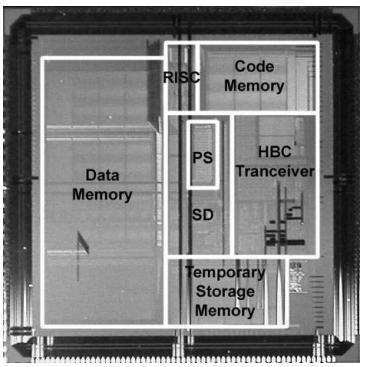

Figure 7. Photograph of the BSN processor

When the system operates with energy-aware module with 16-kHz clock frequency, it consumes 21.6-μW for nodes management. The Shmoo plot in figure 8 shows that the processor can operate up to 11-MHz system bus clock frequency with 0.6V supply voltage. And figure 9 shows its power consumption with various clock frequencies when the supply voltage is fixed to 0.6V. In this implementation, 16-kHz SD frequency and 4.2-MHz system frequency is chosen to support 256-kbps packet bandwidth. The packet bandwidth linearly increases with the SD clock frequency without changing the system design. With 1.7% RISC activation ratio, the processor consumes 24.2-μW average power with 4.2-MIPS performance and 256-kbps packet bandwidth which shows the comparable performance with conventional BSN bandwidth.

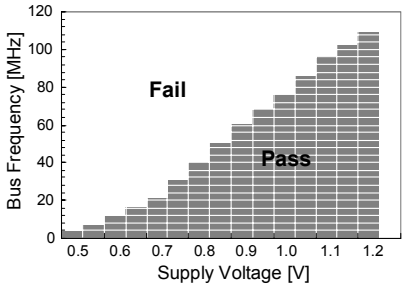

Figure 8. Frequency versus supply voltage plot at body temp.

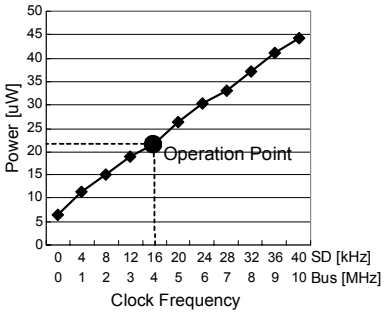

Figure 9. Power Consumption by Clock Frequency with 0.6V VDD

Figure 10 (a) shows the measured data-request signals sent to the four nodes with different periods, 10-seconds for node #1, 20-sec for #3, 30-sec for node #198 and 2-minutes for node #200. Figure 10 (b) are the measured waveforms of SD, especially the data-request sent to the node #198. At the falling edge of the 1sec-clock, internal 8-bit ID_counter increases its value from 1 to 254 to scan the CAM, and PEG generates transmission flag (TXFLAG) and two-words data-request packets (TXPKT) which are the trains of {0x0001, 0x04c6} for node#198. When PEG receives the data (RXPKT) with reception flag (RXFLAG), it moves on to next row by increasing the internal ID_counter. The RXPKT of figure 10 (b) shows that the node #198 sent 5 packet data. Only ID_counter is heavily involved in the signal transaction but it consumes negligible power. The rest of the signals are not precharged or reset to prohibit unnecessary signal transaction. In the figure 10 (b), the data-request of the node #198 is completed in 1ms with 16-kHz SD_clk frequency. If match is not found in the rest of the 1sec-clock, all the signals keep their last values.

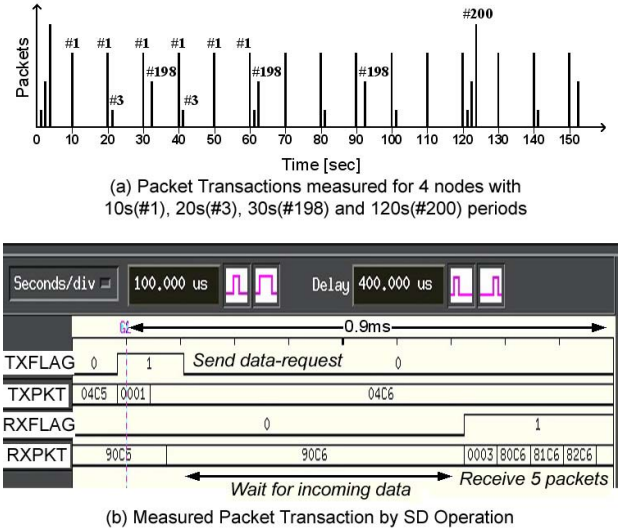

Figure 10. Data-request by SD Operation

V. CONCLUSIONS

The BSN controller with HBC is essential for the implementation of small-size and low-power mobile healthcare system and body monitoring system. The proposed dual-mode system architecture meets the requirements of both power and performance. SD with low voltage TCAM-based PEG and various low-power schemes enable the management of 254 nodes with 16-kHz clock frequency. And the IPEEP scheme activates a RISC quickly from the power-save mode as well as prohibits unnecessary CPU activation which causes the power dissipation. The proposed architecture and schemes were verified by the implementation of HBC control processor for human body monitoring application with 0.18-µm CMOS process. The processor consumes 21.6-µW for node management with 0.6V supply voltage.

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