A Multi-Nodes Human Body Communication Sensor Network Control Processor

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Abstract— **This paper presents a low-power body sensor network (BSN) control processor for human body communication (HBC) with the performance of 254 nodes management. The proposed 'instantaneous program execution with external program counter' scheme provides up to 10-MIPS performance only when it is needed, and the 'TCAM-based period scheduler' manages 254 HBC nodes with 21.6-μW power consumption. They are verified by the implementation of the BSN controller and shows 254 nodes management with 4.2-MIPS performance.**

I. Introduction

The increasing concern about the healthcare and well-being brought up the research of mobile medical service [1] and body sensor network (BSN) so that people can check their own health conditions at any time and any place. In the mobile medical service applications such as remote healthcare monitoring and diagnostics, functions of collecting and analyzing a number of vital signs from different parts of a human body are essential. And ultra low-power consumption is also one of the most crucial requirements for the implantable system which needs surgical operations and cannot be recharged after it is implanted inside human body. Its low-power consumption can reduce the size of battery, resulting in small system form-factor.

Various BSN systems were proposed [2, 3] to implement a mobile healthcare monitoring system. A handheld device like a PDA is used for a network manager or a base-station to manage all the sensor nodes and handle events with its CPU [2]. However, its large form-factor and big battery due to its large power consumption are inconvenient for users to carry with. Although another system with general purpose microcontroller was introduced for low-power operation [3], it can control just 3~4 directly connected sensor nodes, which cannot provide the performance for network management. And most of them use wireless communication which consumes more power than human body communication (HBC) [4]. Other researchs [5, 6] were focused on ultra low-power operation and performance was of secondary importance. One solution to achieve the ultra low-power requirement is to operate the digital logic gates in sub-threshold region.

This paper presents a new hardware architecture and two major schemes for ultra low-power BSN control with high processing performance. An implemented chip for bio medical monitoring shows 24.2-μW average power consumption with 0.6V core voltage, which is the lowest super-threshold region [7] for the performance as high as up to 10-MIPS.

II. Operations For Body Sensor Network Control

Fig. 1 shows the flow-chart of the HBC-BSN control operation. The system starts the whole network components including each node with the system initialization. And it periodically requests the sensor data and stores them in its internal memory for monitoring the status of the human body. If some of the incoming data include warning information or values exceeding pre-defined boundary, it switches to the analysis routine or therapy routine to resolve the problem.

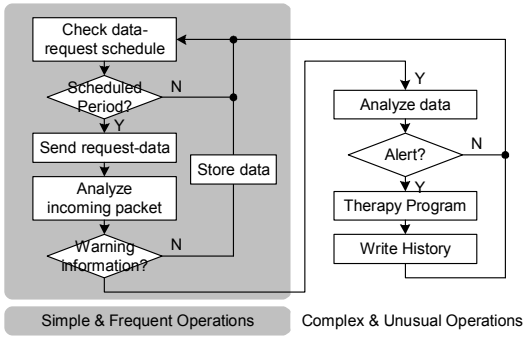


Fig. 1. BSN Operation Flow-chart

Such operations can be classified into two operation groups: group 1 - 'simple but frequently occurring operations' such as data-request with scheduled period, and group 2 - 'complex but unusually occurring operations' such as alert handling in the Fig. 1. Operations of group 1 occur in real-time to gather the sensor data, and the period of the data-request depends on the characteristics of the sensor. For example, a body temperature should be gathered every 2-minutes while a blood pressure should be checked three times a day. From the view point of CPU clock, such period is too long to count, and counting the period by using the CPU is waste of performance and power. Operations of group 2 occur when incoming data has abnormal condition or exceeds the pre-defined safety range, and needs high computing performance to execute

analysis/therapy programs. Conventional architecture with general purpose CPUs [8] uses interrupt service routines (ISR) to handle exceptions. However, they have only limited number of interrupt resources to allocate to each node. Although the number can be extended by using interrupt controller, extra operations for interrupt request (IRQ) analysis are required and so are the additional execution time and power consumption.

In conventional architectures, operations of both groups were handled by a single general-purpose CPU which cannot provide any optimized operations to any of the groups. The proposed architecture, meanwhile, is divided into two operation modes, MANAGE mode for operation group 1 and ALERT mode for operation group 2, to manage 254 BSN nodes with 21.6-µW power consumption. A schedule director (SD) with ternary content addressable memory (TCAM)-based period scheduler (PS) manages the issuing period for each node with 16-kHz clock frequency. The instantaneous program execution with external program counter (IPEEP) scheme activates the CPU only when it is needed.

III. Dual-Mode BSN Control Processor

The proposed system consists of two modules, the modules for MANAGE mode and ALERT mode, as shown in Fig. 2. The RISC is the master of the system bus and memory blocks, but it is activated by SD. For periodic data request operations, only the MANAGE module is activated and SD itself controls the whole system. When complex jobs should be executed, SD wakes up the RISC. Then the ALERT module is activated and the RISC controls the whole system.

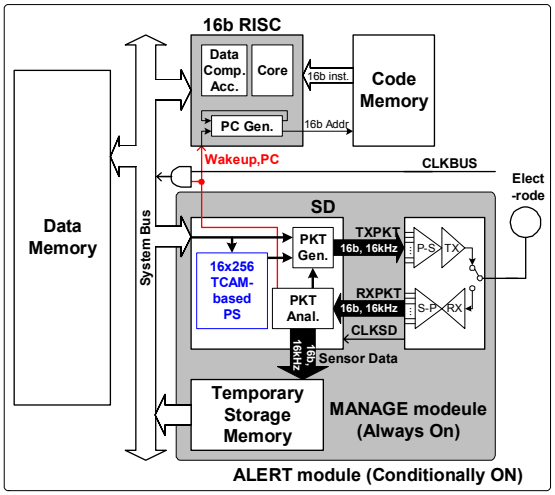


Fig. 2. Dual-mode BSN Control Processor

Average power consumption of the entire system depends on the activation ratio of the RISC which consumes most of the system power. Assuming that the RISC is activated one minute per every hour, the activation ratio is just 1.7% and the whole system power consumption can be dramatically reduced by selectively activating the ALERT module only when it is needed. The IPEEP scheme activates the ALERT module without operational overhead such as register backup and restoration. Due to the proposed TCAM-based PS, SD works with as low as 16-kHz clock frequency to reduce the number of signal transitions and corresponding charging and discharging energy consumption.

A. *Instantaneous Program Execution with External Program Counter (IPEEP)*

Two kinds of resets exist in the proposed IPEEP scheme, resets by external reset-switch and by SD. With the system start-up, the RISC executes a program starting from the address 0, in which generally the system initialization code or boot-up code is stored. With the IPEEP scheme, end of the boot-up code includes the CPU power-save mode instruction so that the RISC cuts off its power autonomously to reduce unnecessary power dissipation. When SD wakes up the RISC, it provides an appropriate program counter (PC) value and the RISC executes a program starting from the address pointed by the PC. Since internal registers of the RISC is initialized by the same way as the conventional reset sequence, additional time for restoring internal registers or IRQ handling is not required. With the IPEEP scheme, large number of interrupt handling is achieved without interrupt control IP and ISR. For the realization of IPEEP scheme, the PC generation block of the RISC has two PC inputs, internal PC and external PC. And SD generates the wake-up signal by analyzing the incoming data packets.

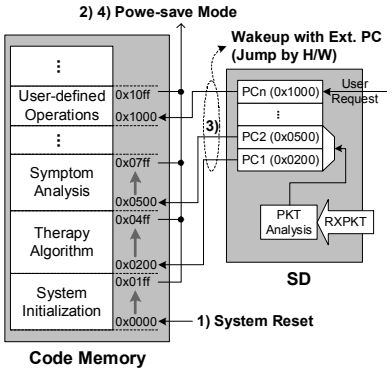


Fig. 3. Program Execution with IPEEP Scheme

Fig. 3 shows an example of the memory map with IPEEP scheme for a healthcare monitoring system. With the system reset (1), the initialization code sets all of the BSN system including each node and it goes to power-save mode (2), and SD manages all the sensor nodes. When SD gets abnormal sensor data, it wakes up the RISC with PC2 (3) and the RISC executes symptom analysis program. And when SD gets alert signal from a sensor node, it wakes up the RISC with PC1 so that the RISC executes therapy program. After the RISC completes the program execution, it goes to the power-save mode and cuts off its power (4).

B. *SD with TCAM-based Period Scheduler*

SD manages outgoing data-request/command packets and incoming data from each BSN node. The TCAM-based PS issues and generates the data-request packets with up to 254 independent periods for BSN nodes, while conventional system issues them using hardware timers which consume considerable power and silicon area. It is one of the reasons why conventional CPU supports only limited number of timers.

In the CAM operation, most of energy is consumed for search operation. In this application, however, search operation occurs just once a second and it finds out the ID of the nodes to be issued by enabling corresponding match lines (ML). The search results are issued in order, from ML1 to MLn with 16-kHz clock frequency as shown in Fig. 4 (a). If a ML is enabled, the request-generation block (REQ.Gen.) shown in Fig. 4 (b) issues the data-request packet by using the ML number as the node number. And if the ML is disabled, it skips the packet generation and checks next ML. Fig. 5 compares the energy consumption of the conventional hardware timer and the proposed PS with three values of TCAM match ratio. If the CAM searches 10 match lines out of 256 words every search cycle, the ratio becomes 4%. It shows that the TCAM-based PS consumes 8x less energy for management of 100 nodes.

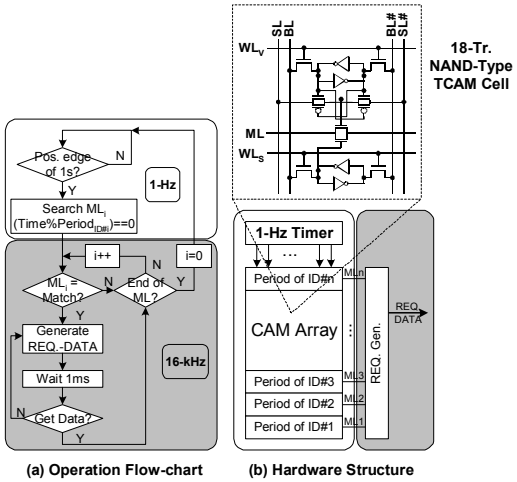


Fig. 4. TCAM-based PS

The proposed 18-Tr. NAND-type TCAM cell for low voltage search operation is shown in Fig. 4(b). Although it has two more pMOS transistors compared with previous NAND-type TCAM cell [9], the transmission gate passes the match signal without Vth-drop, which enables 0.6V supply voltage search operation.

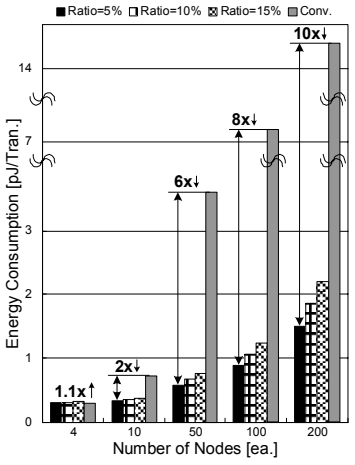


Fig. 5. Energy Consumption for Scheduling Nodes

IV. IMPLEMENTATION

The proposed schemes are implemented for an ultra low-power HBC BSN control processor as shown in Fig. 6. The 25mm^2 chip consists of a 16bit RISC with IPEEP scheme, SD, three application-specific memory blocks and the HBC transceiver. Data I/O interface of SD is designed to communicate with simplified packet structure so that it can easily connect with HBC transceiver. The processor is implemented with 0.18-μm CMOS logic process and it works with 0.6V core voltage.

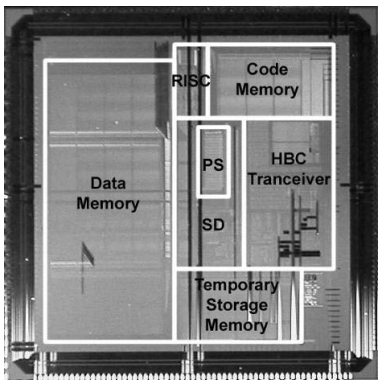


Fig. 6. Photograph of the BSN processor

Fig. 7 shows the measured waveform of TCAM match operation with 0.6V supply voltage. The proposed TCAM block requires 45-ns for the match results evaluation (Eval.) operation and 12-ns for match line precharge (PCG) operation, which values are enough for 16-kHz clock operation. The block can work faster than 16-kHz clock to increase the number of period information to be scheduled, without changing the design for faster operation.

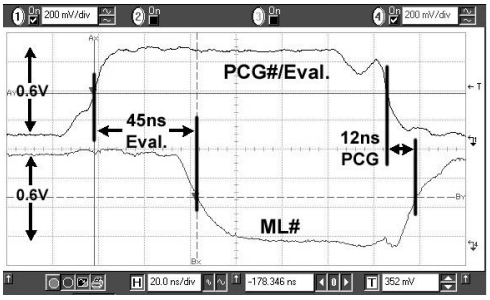
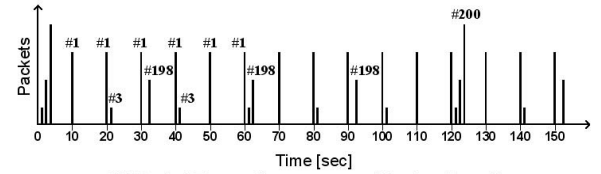


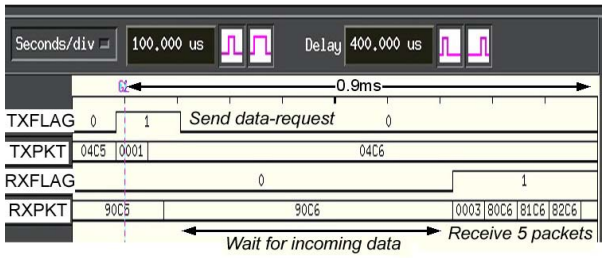
Fig. 7. Measured Waveform of PS operation with 0.6V VDD

Fig. 8 (a) shows the measured data-request signals sent to four nodes with different periods, 10-seconds for node #1, 20-sec for #3, 30-sec for node #198 and 2-minutes for node #200. Fig. 8 (b) is the measured waveforms of SD, especially the data-request sent to the node #198. At the falling edge of the 1sec-clock, internal 8-bit ID_counter increases its value from 1 to 254 to scan the CAM, and PS generates transmission flag (TXFLAG) and two-words data-request packets (TXPKT) which are the trains of {0x0001, 0x04c6} for node#198. When PS receives the data (RXPKT) with reception flag (RXFLAG), it moves on to next row by increasing the internal ID_counter. The RXPKT of Fig. 8 (b) shows that the node #198 sent 5 packet data. Only ID_counter is heavily involved in the signal

transaction but it consumes negligible power. The rest of the signals are not precharged or reset to prohibit unnecessary signal transaction. In the Fig. 8 (b), the data-request of the node #198 is completed in 1ms with 16-kHz SD_clk frequency. If match is not found in the rest of the 1sec-clock, all the signals keep their last values.



(a) Packet Transactions measured for 4 nodes with 10s(#1), 20s(#3), 30s(#198) and 120s(#200) periods



(b) Measured Packet Transaction by SD Operation

Fig. 8. Data-request by SD Operation

When the system operates with MANAGE module with 16-kHz clock frequency, it consumes 21.6-µW for nodes management. The Shmoo plot in Fig. 9 shows that the processor can operate up to 11-MHz system bus clock frequency with 0.6V supply voltage. And Fig. 10 shows its power consumption with various clock frequencies when the supply voltage is fixed to 0.6V. In this implementation, 16-kHz SD frequency and 4.2-MHz system frequency is chosen to support 256-kbps packet bandwidth. The packet bandwidth linearly increases with the SD clock frequency without changing the system design. With 1.7% RISC activation ratio, the processor consumes 24.2-µW average power with 4.2-MIPS performance and 256-kbps packet bandwidth which shows the comparable performance with conventional BSN bandwidth.

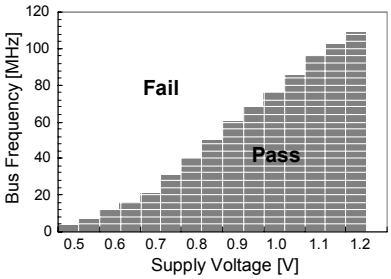


Fig. 9. Frequency versus supply voltage plot at body temp.

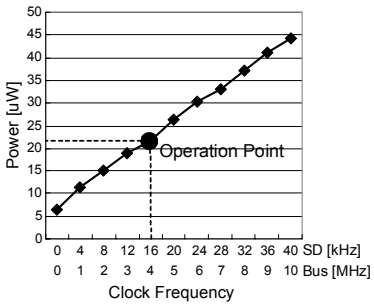


Fig. 10. Power Consumption with Clock Frequency

V. CONCLUSIONS

HBC BSN control processor with high computing performance is essential for the implementation of low-power mobile healthcare system and body monitoring system. The proposed control processor meets the requirements of both power and performance. SD with low voltage TCAM-based PS and various low-power schemes enable the management of 254 nodes with 16-kHz clock frequency. The IPEEP scheme activates RISC quickly from power-save mode and prohibits unnecessary CPU activation which causes the energy dissipation. The proposed architecture and schemes were verified by the implementation of HBC control processor for human body monitoring application with 0.18-µm CMOS process. The processor consumes 21.6-µW for node management and 24.2-µW for alert handling with 0.6V supply voltage.

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