A 0.6pJ/b 3Gb/s/ch Transceiver in 0.18 μm CMOS for 10mm On-chip Interconnects

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***Abstract*—This paper presents a high speed and low energy transceiver for 10mm long minimum width on-chip global interconnects. To improve the link bandwidth, the transmitter employs a capacitive-resistive pre-emphasis technique and the receiver employs the AC-coupled Resistive Feedback Inverter (RFI) de-emphasis technique. Exploiting two emphasis techniques, the proposed interconnect achieves 1.26GHz bandwidth which is 20 times improved compared to conventional link. As a result, it achieves error-free 3Gb/s data rate and consumes less than 0.6pJ/b during transmission by using low-swing and pulse signaling. The test chip is designed using 1.8V 0.18 μm 6M CMOS technology.**

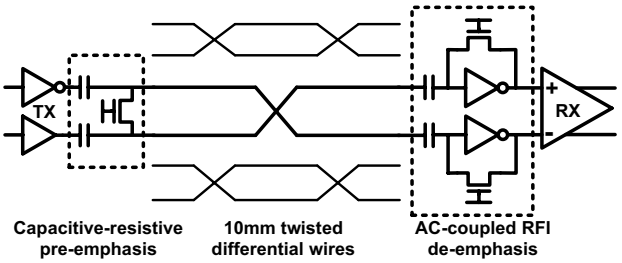

Figure 1. The overview of proposed transceiver

I. INTRODUCTION

As global interconnects are becoming a speed, power and reliability design issue for digital systems, the on-chip communication is getting more attention [1]. Especially the process scales down to deep sub-micron scale, the RC delay of wires become more and more critical because it is relatively less improved than the gate delay [2]. Furthermore, as the size of VLSI design increases, the uses of longer wires for global interconnects are frequently occurred.

In the global on-chip interconnects, wire bandwidth is the very critical metric of on-chip communication performance. The small bandwidth of interconnect causes inter symbol interference (ISI), which is primary limitation to the achievable data rate. As the length of wire increases, the bandwidth of wire is significantly limited by its high resistance and capacitance. Wire delay, which is inversely proportion to wire bandwidth, also grows quadratically. Therefore, to increase achievable data rate and enhance on-chip communication performance the bandwidth of interconnects should be extended.

Traditionally, a general solution to solve the limited interconnect bandwidth is the use of repeated buffers, which make the interconnect latency linear with wire length. However it consumes a considerable amount of area and power. Another solution is to use microstrip on-chip transmission lines [3]. They offer high bandwidth and near-speed-of-light latency, exploiting the LC regime of wide wires, but consume significant interconnect area. Recent researches [4-6] increase the achievable data rate at the cost of high static power consumption. The capacitive pre-emphasis technique [7-8] increases the wire bandwidth with low energy consumption. It drives long wire through series capacitor and results effective increase of bandwidth and low voltage swing. However, the bandwidth of capacitively driven wire is limited to a 3X gain compared to the conventional wire which has 63MHz bandwidth. To improve the bandwidth beyond this limitation, we propose capacitive-resistive pre-emphasis and an AC-coupled Resistive Feedback Inverter (RFI) de-emphasis technique as shown in Fig.1. Exploiting parallel resistor added to series capacitor, capacitive-resistively driven wire offers 8 times improved bandwidth gain compared to conventional wire, and a 2.5X gain compared to capacitively driven wire. AC-coupled RFI de-emphasis technique increases wire bandwidth and achievable data rate further. As a result, two proposed techniques offer 1.26GHz bandwidth which is able to achieve 3Gb/s data rate and this is 20 times improved compared to conventional wire. And their low voltage swing and pulse signaling enables energy efficient data transfer in global interconnects. Implemented transceiver in 0.18μm process consumes only 0.6pJ to transfer 1 bit in 10mm wire.

This paper is organized as follows. Chapter II explains proposed pre-emphasis and de-emphasis technique in detail. Chapter III describes the implementation of the transceiver. The results of implemented transceiver will be shown in chapter IV. Lastly, conclusion of this paper will be made in chapter V.

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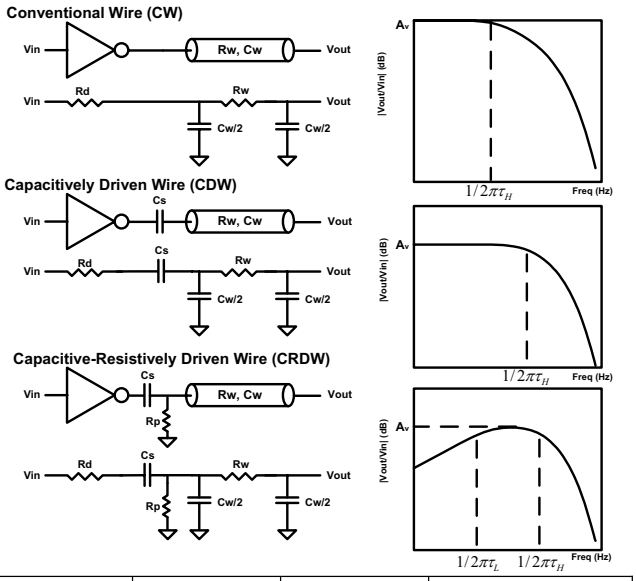
II. EMPHASIS TECHNIQUES

A. Capacitive-resistive pre-emphasis

Fig. 2 shows the simple models of different pre-emphasis schemes and their transfer functions. There are conventional wire (CW), capacitively driven wire (CDW) and capacitive-resistively driven wire (CRDW). Interconnects are modeled by simple π-wire model which gives circuit intuition and enables quick analysis. We assume that the transmitter drives wire by its source impedance R_d, and the termination of the receiver side is the capacitive load from a gate. Because it is extremely small compared to the wire capacitance C_w, thus we ignore this as shown in Fig. 2. In CRDW, the transmitter drives only C_S not whole wire capacitance C_W by inserting series capacitance Cs in the wire. In the same manner, newly added parallel resistor R_P reduces the wire resistance R_W that transmitter drives. Therefore, driving a wire using C_S and R_P both is much faster than driving a wire using only C_S. Analysis about time constants and voltage gain for three pre-emphasis schemes are described in Fig. 2. CRDW reduces signal swing A_V through a capacitive and resistive divider and introduces a zero-poles pair that pre-emphasizes the transmitted signal. It also boosts the wire bandwidth ($\frac{1}{2\pi\tau_H} - \frac{1}{2\pi\tau_L}$) more than previous CDW. Assuming that the transmitter output impedance R_d is small enough, we can ignore R_d term in the analysis results. Then, the time constant τ_H of CDW becomes a half of CW, and this leads the bandwidth of CDW to be the only two times of CW. On the other hand, a CRDW reduces time constant in factor of $\frac{2R_W}{R_P//R_W}$ which can be larger than 2. Therefore it can increase the wire bandwidth by the ratio of the resistance value R_P and R_W. This indicates that CRDW provides more effective way to increase wire bandwidth and reduce wire delay than CDW. For example, at 100mV low-swing signaling in V_{DD} of 1.8V, in CDW case, we can choose C_S as $\frac{1}{20}C_W$ offering 2BW. On the other hand, in CRDW case, we can choose C_S as $\frac{1}{8}C_W$ and R_P as $\frac{1}{4}R_W$ offering 8BW, where BW means conventional wire bandwidth. To verify efficiency of CRDW more accurately, we simulate AC response of distributed wire model. Fig. 3 shows the simulated transfer functions of a 10mm long minimum-width interconnects, placed in metal 4, which have a total distributed resistance of 2.8kΩ and a capacitance of 2pF. In Fig. 3, conventional case with an inverter used as both a transmitter and a receiver has only 63MHz bandwidth. A CDW increases the bandwidth up to 3X, and a CRDW up to 8X at 50mV voltage swing. The CRDW is faster and has larger bandwidth than CDW because the combination of C_S and R_P creates a wire from the transmitter to the receiver with a band-pass response. The parallel resistor and series capacitor filter out the low-frequency components thereby effecting more pre-emphasis effect, which speeds up wire delay and reducing ISI. Fig. 4 shows the implementation of parallel resistor R_P. It can be simply implemented by a connecting transistor operated in the triode region. Two differential wires are acting as a virtual ground and the effective resistance value becomes twice. This parallel resistance also has a benefit to the stabilization of differential wires DC bias balance.



Pre-emphasis scheme	CW	CDW	CDRW
τ_L	∞	∞	$(R_P + R_P//R_W)\,C_W$
τ_H	$\frac{R_W C_W}{2}$	$R_d C_S + \frac{R_W C_W}{4}$	$R_d C_S + \frac{(R_P//R_W)\,C_W}{4}$
A_V	1	$\frac{C_S}{C_S + C_W}$	$\frac{C_S}{C_S + C_W}\,\frac{R_P + R_P//R_W}{R_P + R_W}$

Figure 2. Simple model of different pre-emphasis schemes and their transfer functions

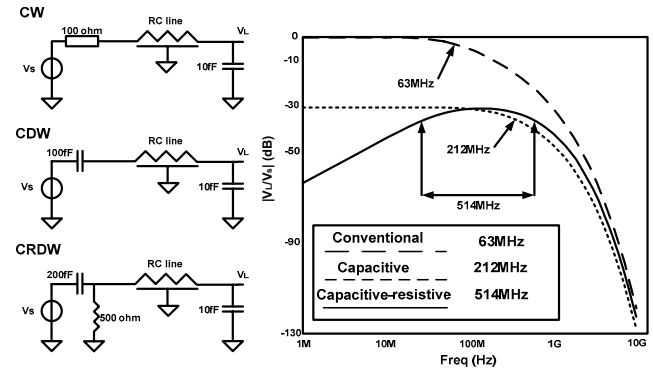


Figure 3. Transfer function with distributed wire (R=2.8 kΩ and C= 2pF)

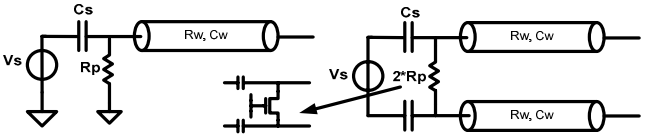


Figure 4. Implementation of parallel resistor

B. AC-coupled RFI de-emphasis

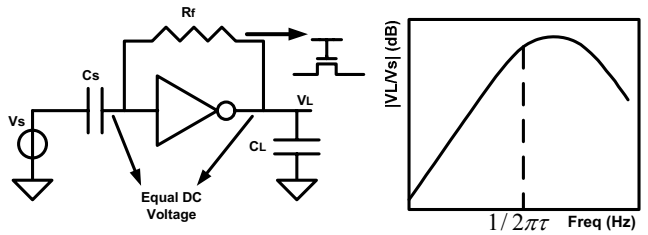


Figure 5. AC coupled RFI and its transfer function

To improve wire bandwidth and achievable data rate further, we propose AC-coupled RFI at the receiver side. Fig. 5 shows an inverter with negative feedback resistor R_f and series capacitor C_S. With a small R_f (< 20 kΩ), the amount of feedback is large, therefore RFI structure can be used as not amplifier but bandwidth booster. The AC-coupled RFI de-emphasizes the low frequency components, thereby, reducing ISI and increasing wire bandwidth as shown in Fig. 5. Assume that R_f is small, then time constant τ is given as (1),

$$\tau = R_f \left(\frac{C_S C_L}{C_S + C_L}\right) \quad (1)$$

The C_S also isolates receiver side from interconnects. The R_f can be simply implemented by transistor operating in deep triode mode and, with negative feedback, enable inverter to bias itself. Therefore, the RFI structure has the inverter continuously turn on, consuming small static current. The AC-coupled RFI de-emphasis technique used in combination with capacitive-resistive pre-emphasis technique consumes almost no extra power, improved wire bandwidth up to 1.26GHz. This is 20 times improved compared to conventional wire.

III. Tranceiver Circuit Imlementation

To reduce the overall crosstalk between wires, differential interconnects are frequently used [9]. Furthermore, to cancel neighbor-to-neighbor crosstalk between channels in bus, one twist is placed at 50% of the length in the even channels and two twists are placed at 25% and 75% in the uneven channels. The transmitter is implemented by three cascade inverter to transmit NRZ signal. Series capacitors are implemented using NMOS capacitor. With only series capacitors, the DC voltage of the interconnect is not defined well because there is no DC path to one of the supplies. Because of two AC-coupled wires, the wires and receiver inputs require a voltage bias. To control interconnect side DC voltage, a load resistor R_L and a transconductance G_m controlled by V_{in} [8] are used as shown in Fig. 6. If a small G_m and a large R_L are chosen, the static current is kept small. As shown in Fig. 6. G_m and R_L are implemented with MOS transistors. The area consumed by C_{S1} is $4.6 \times 4.6\,\mu m^2$ for 200fF. The total area of the differential transmitter is $520\mu m^2$. The signals, with a voltage swing of 100mV, are chosen close to V_{DD} of 1.8V, because the capacitance of the NMOS transistor is highest for a high gate-source voltage. For receiver side, RFI bias itself close to $V_{DD}/2$. The C_{S2} also consumes relatively small area which is $2.4 \times 2.4\,\mu m^2$ for 50fF. The receiver is implemented by a

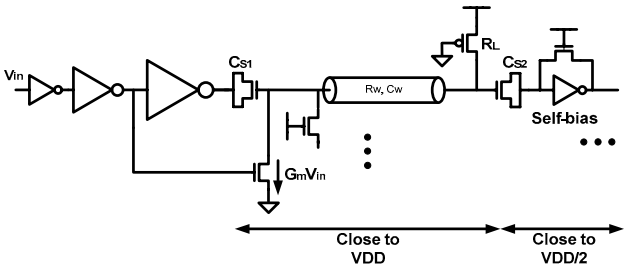


Figure 6. NMOS series capacitors and wires bias

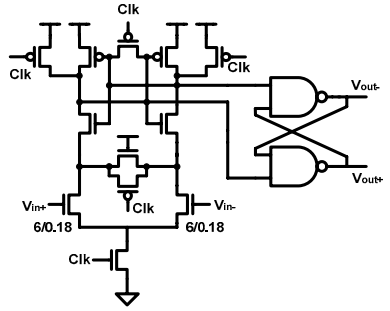


Figure 7. Clocked comparator receiver

clocked comparator, sized for a small offset as shown in Fig. 7. The receiver recovers the NRZ data from the low-swing pulse signal. The total area of the receiver is $340\mu m^2$.

IV. Implementation Results

The proposed CDRW and RFI scheme and previous CDW use low-swing and pulse signaling as a pre-emphasis effect. In contrast to NRZ signaling used in full-swing repeated

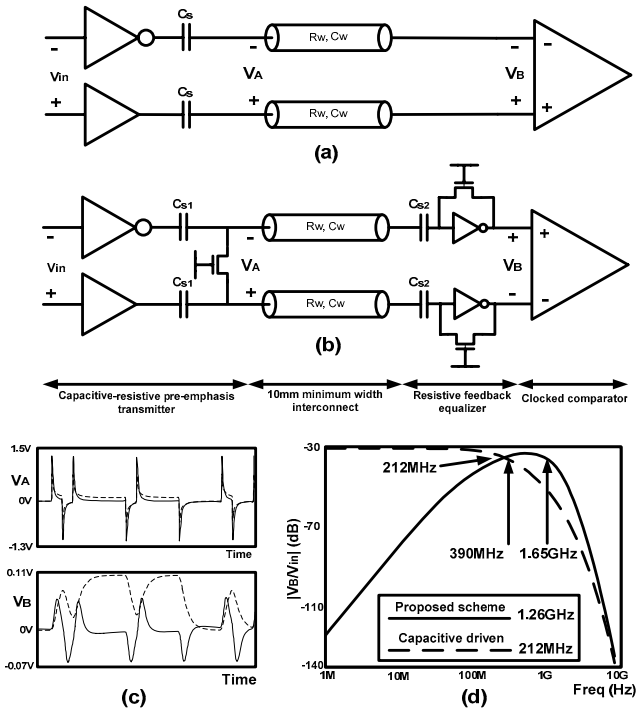


Figure 8. (a) CDW overview (b) Proposed CDRW and RFI scheme overview (c) Transient waveforms (d) frequency responses

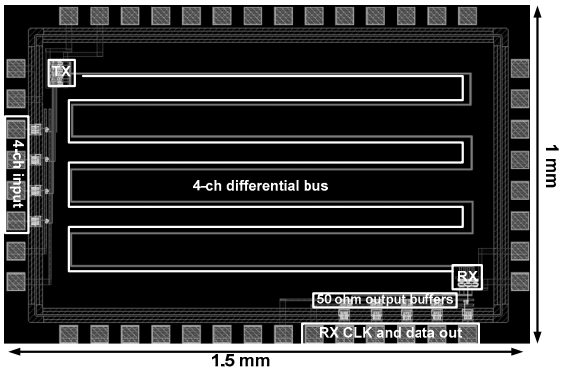


Figure 9. The layout photograph of the test chip

buffer, pulse signaling and low-swing signaling significantly minimize power dissipation on interconnects. Fig. 8 shows the performance comparison between CDW and proposed wire. In Fig. 8 (c), The V_A waveforms show the pre-emphasis spikes of CDW and proposed wire. They convert the NRZ data into pulse signals at the data transitions. Compared to the waveform of CDW, the waveform of proposed wire has larger pre-emphasis spike because it blocks the low frequency components further by exploiting parallel resistance. Therefore, large pre-emphasis spike of proposed wire charges the wire fast and makes wire delay short. As a result, short wire delay increases the bandwidth further. The V_B waveform of Fig. 8(c) shows 100mV differential signals at the receiver side. As you see in the waveforms, the low frequency ingredients of proposed wire waveform are de-emphasized by AC-coupled RFI circuit. This results in reducing ISI and increase achievable data rate. As a result, the latency of CRDW is decreased to 240ps, while the latency of CDW is 760ps. The speed-up of proposed wire can be proved from the wire's frequency responses shown in Fig. 8 (d). They show the bandwidth of CRDW is increased to 1.26GHz which is 6.1 times improved compared to that the bandwidth of CDW is limited to 212MHz.

To verify efficiency of proposed wire, we design the test chip. Fig. 9 shows the test chip layout with 4 channel 10mm-long minimum width interconnects. The receiver clock is generated externally to adapt its phase to the transmitted data of the receiver side. Fig. 10 shows simulated eye-diagrams at the 50 **Ω** matched output at 1Gb/s, 2Gb/s and 3Gb/s data rate. The eye-opening of each diagram results 91%, 81% and 70% for 1Gb/s, 2Gb/s and 3Gb/s data rate. Simulation results verify we can achieve a 3Gb/s error-free on chip communication. In Fig. 11, the simulated energy per bit is plotted as a function of transition probability. With a random data pattern at 3Gb/s, only 0.6pJ/b is dissipated which is significantly reduced compared to previous works.

V. CONCLUSION

We present a high speed and low energy transceiver for 10mm minimum width wires in 0.18μm CMOS process. While the conventional wire is RC-limited to 63MHz, proposed capacitive-resistive pre-emphasis with AC-coupled RFI de-emphasis increases wire bandwidth up to 1.26GHz. These two techniques also enable interconnects to use low-swing and pulse signaling, which saves energy significantly in data transfer. As a result, the achievable data rate increases to 3Gb/s and consumes only 0.6pJ/b.

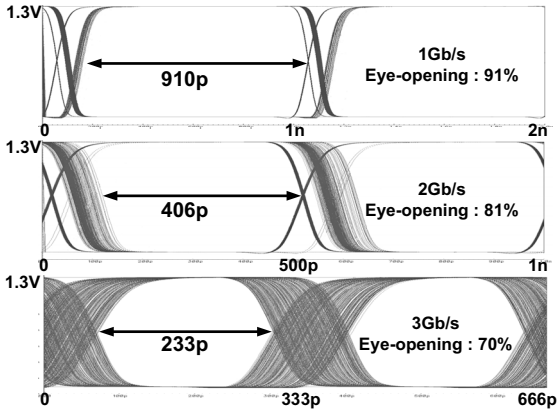


Figure 10. Simulated eye-diagrams at 50 **Ω** matched output

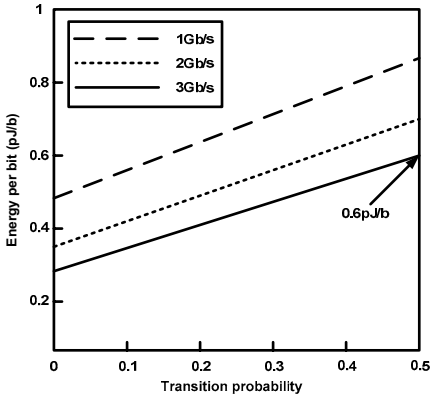


Figure 11. . Simulated energy consumption as the transition probability

REFERENCES

[1] R. Ho, K. Mai, and M. Horowitz, "The Future of Wires," Proc. IEEE, vol.89, no. 4, pp. 490-504, Apr., 2001.

[2] International Technology Roadmap for Semiconductors [Online]. Available: http://public.itrs.net

[3] A. Jose, G. Patounakis, and K. Shepard, "Pulsed Current-Mode Signaling for Nearly Speed-of-Light Intrachip Communication," IEEE J.Solid State Circuits, vol. 41, no. 4, pp. 772-780, Apr., 2006.

[4] D. Schinkel, E. Mensink, E. A. M. Klumperink, "A 3-Gb/s/ch Transceiver for 10-mm Uninterrupted RC-limited Global On-Chip Interconnects," IEEE J. Solid-State Circuits, vol. 41, no. 1, pp. 297-306, Jan., 2006.

[5] A. P. Jose, and K. L. Shepard, "Distributed Loss Compensation for Low-Latency On-Chip Interconnects," ISSCC Dig. Tech. Papers, pp. 516-517, Feb., 2006.

[6] L. Zhang, J. Wilson, R. Bashirullah, "Driver Pre-Emphasis Techniques for On-Chip Global Buses," ISLPED, pp. 186-191, Aug., 2005.

[7] R. Ho, T. Ono, F.Liu, R.Hopkins, A. Chow, J. Schauer and R. Drost, "High-Speed and Low-Energy Capacitively-Driven On-Chip Wires," ISSCC Dig. Tech. Paper, pp.412-413, Feb., 2007.

[8] E. Mensink, D. Schinkel, E. Klumperink, E. Tuijl, B. Nauta, "A 0.28pJ/b 2Gb/s/ch Transceiver in 90nm CMOS for 10mm On-Chip Interconnects," ISSCC Dig. Tech. Paper, pp.414-415, Feb., 2007.

[9] Y. Massoud, J. Kawa, D. MacMillen and J. White, "Modeling and Analysis of Differential Signaling for Minimizing Inductive Cross-Talk," Proc. DAC, pp. 804-809, June, 2001.